The Improve of Pixel Design and Circuit Signal on Short Time Image Sticking for Flexible AMOLED

Xia Tang*, Yue Wei, Tingliang Liu**, Yonglin Guo**, Guoqiang Yang**, Xu Yang**, Lei Deng**, Yi Zhang**, Yongyi Fu*****

***Chengdu BOE Optoelectronics Technology CO., LTD**

Abstract

The simulation model of short time image sticking (IS-ST) of AMOLED displays was established. The impact of black plane circuit pixel design and work voltage had been studied. Pixel with good simulated IS-ST had been optimized by decreasing the parasitic capacitance of M3 node and VDD line (C_M3_VDD) and the Length of switch TFT (TFT L). And IS-ST also can be improved by Reducing the L0 gray data voltage (VGMP) and Vinit voltage (Vinit). All the solutions proposed above had been applied on our AMOLED display product, thus reaching the achievement that IS-ST value decreases from 8 JNCD to 5.5JNCD at 0s.

Author Keywords

Short time image sticking, parasitic capacitance, TFT length, VGMP, Vinit

1. Introduction

AMOLED displays have been studied for decades, due to their wide viewing angle, fast response time, low cost and thinness [1]. They are already being adopted as displays for small size applications such as mobile phone and wearable products. Low temperature polysilicon (LTPS) TFTs have been widely used as pixel transistor because of their high mobility, high reliability as well as their capability for integration on glass subsite. With the upgrading of LTPS-OLED display technology, customer have higher expectation on OLED display's image quality. The OLED display will be facing more challenges while the application of novel technologies such as high refresh rate and DC dimming have be broadly used.

There are several image quality problems, image sticking, crosstalk, long range uniformity (LRU) and Mura, for example. Among them one of the critical issues is the image sticking. It is also called residual image. Image sticking is divided into long time image sticking and short time image sticking (IS-ST). It is understandable that long time image sticking occurs in the case that the diodes are degraded with emitting time. However IS-ST is a recoverable image sticking, such that the previous display image remains in the subsequent image for a time ranging from 5s to 70s. Over the years, solutions of the IS-ST have been carried out actively. Most of the researchers conclude that the cause of the IS-ST is proven to be the hysteresis of the driving TFT in the black plane circuit. The IS-ST can be eliminated by reducing the hysteresis level. The hysteresis is explained by carrier trapping and de-trapping at the interface region of the channel. The hysteresis of p-channel LTPS TFTs is more sensitive by the variation of the interfacial defect state.

We focus on the effects of pixel design and work voltage of black plane circuit, including the C_M3_VDD, the TFT L, the VGMP and the Vinit.

2. Simulation model

IS-ST is tested as follows:

(1) Display the L48 gray pattern in full screen, as shown in figure1 (a).

(2) Switch to the black and white pattern and keep it for several seconds, as shown in figure1 (b).

(3) Switch to the L48 gray pattern. Use the CCD equipment to measure the luminance of the red frame A and B, which is recorded as $I(t)_A$ and $I(t)_B$ respectively, as shown in figure1(c). The test is performed dozens of times at an interval of 1s.

(4) Calculate the JNCD by formula (1).

$$JNCD = \frac{I(t)_A - I(t)_B}{(I(t)_A + I(t)_B) * 0.004} \quad (1)$$

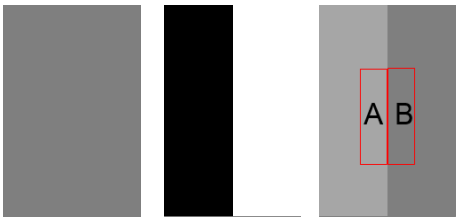


Fig. 1. The test pictures of IS-ST: (a) L48 gray pattern, (b) black and white pattern, (c) calculation area of L48 gray pattern.

Figure2 shows the IS-ST curve tested by CCD device. The horizontal axis is test times, while, the vertical axis is luminance. The two lines respect the luminance of red frame A and B as shown in Figure 1 (c).

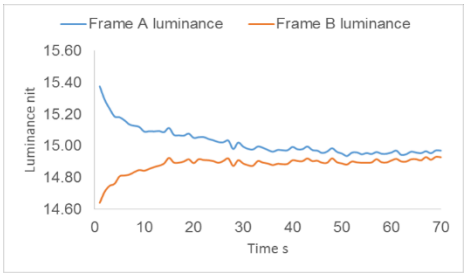


Fig. 2. The IS-ST curve tested by CCD device

According to the above test method, a similar simulation

method is established. Two same pixels are included in the model with same cap and TFT width and length, which are named as pixel A and pixel B. The Data voltage of L255 gray recorded as V1 is written into pixel A and changed to V0 to change to L48 gray after 10 seconds. Similarly, The Data voltage of L0 gray recorded as V2 is written into pixel A and changed to V0 to change to L48 gray after 10 seconds. Finally, the current of pixel A and B would be obtained as I1 and I2, which are different due to the TFT hysteresis. The simulation formula was established to replace the complex test formula, which calculating the difference of center current as follows [2]:

$$\Delta Ids = \frac{abs(I1 - I2)}{abs(I1 + I2)} * 100\% \quad (2)$$

3. Results

(a) Simulation results: The pixel layout is shown in figure3, including data line, scan line, the VDD signal and the Vinit signal. The parasitic capacitance of M3 node and VDD signal line (C_M3_VDD) and gate electrode of driving TFT (M1 node) are marked. Figure4 shows the pixel current simulation change of C_M3_VDD, and A)-C) correspond to the C_M3_VDD of 8.3fF, 6fF and 4.2fF separately. The red line and green line are the current of pixel A and pixel B respectively, and the horizontal axis is times. After 10 seconds, the pixel current is changed when V1 and V2 are change to V0. Enlarging the area a-c, the trend of I1 (green line) and I2 (red line) can be clearly observed as shown in a)-c). This is similar to the IS-ST curve tested by CCD. It is evident that the differences between I1 and I2 reduce over time, and they will be equal finally due to the recovery of TFT hysteresis. The difference between I1 and I2 is decreased as the C_M3_VDD falls. In the simulation, I1 and I2 at 0s time were selected to calculate to obtain the simulation ΔIds according to the formula (2). In Figure5 (a), C_M3_VDD-ΔIds curve has been acquired. The ΔIds decreases from 1.5%→1.42%→1.33% as the C_M3_VDD falls from 8.3fF→6fF→4.2fF. In other word, the ΔIds decreases about 6% when the C_M3_VDD declines about 2fF.

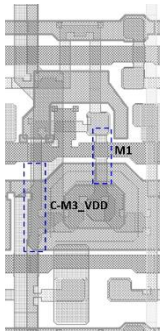


Fig. 3. The schematic of Pixel Layout，especial the C_M3_VDD and the M1 node

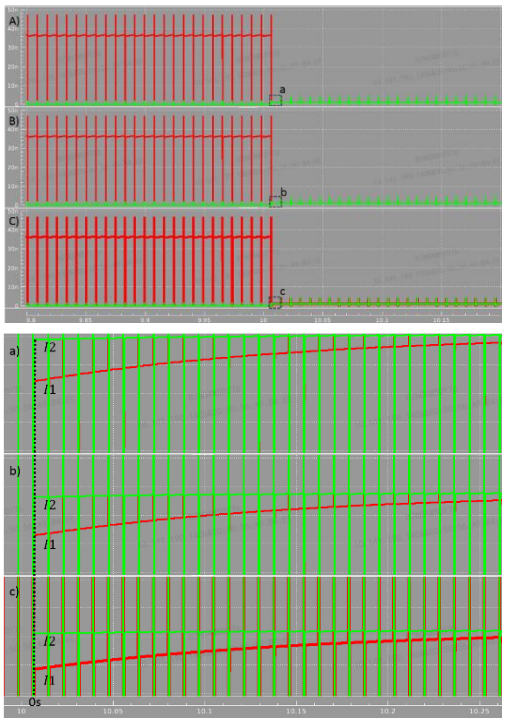
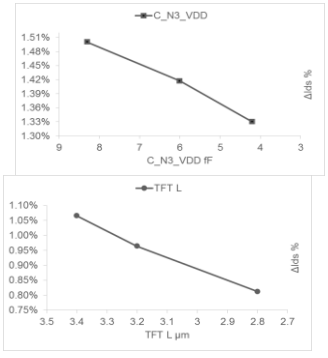
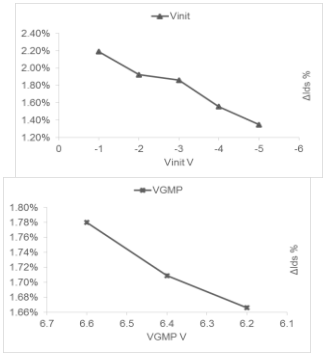


Fig. 4. The pixel current simulation change of C_M3_VDD

In addition, single factor design is used in the study of the impact of TFT L, Vinit, and VGMP on ΔIds in simulation mode. For TFT L, we take 3.4μm, 3.2μm, 2.8μm as the single factor to simulation. For Vinit, we take -1v to -5v to simulation with an interval of 1V. For VGMP, we take 6.6v to 6.2v to simulation with an interval of 0.2v. In figure5 (b)-(d), TFT L-ΔIds, Vinit-ΔIds, and VGMP-ΔIds curves are exhibited. The ΔIds declines about 9% when the TFT L decreases 0.2μm. The ΔIds declines about 14% as the Vinit decreases 1V and declines about 3% as the VGMP decreases 0.2v.



(a) (b)



(b) (d)

Fig. 5. The impact of C_M3_VDD(a), TFT L(b), Vinit(c), VGMP(d) on ΔIds

(b) How the simulated factors improve the IS-ST :

(1) IS-ST can be modified by lowering the C_M3_VDD, because the charging rate of circuit is greatly increased by decreasing the parasitic capacitance, which brings about the small potential difference (△M1) at gate electrode of driving TFT (M1 node) between L255 gray changed to L48 gray and L0 gray changed to L48 gray.

(2) Similarly, TFT with smaller channel length has a better TFT character with a higher Ion， which makes the charging rate increased, leading to a smaller △M1. On the other hand, the smaller △M1 also can be achieved by reducing the influence of Gate Timing Jump on the N1 node potential through decreasing the TFT L.

(3) However, for the Vinit and the VGMP, the mechanism for IS-ST improvement is different. It is inferred that the charge current increases as the Vinit reduces, resulting in faster recovery of the charge trapped. As the VGMP reduces, the difference of the charge trapped between L255 gray changed to L48 gray and L0 gray changed to L48 gray decreases. Thus these two situations bring to a smaller hysteresis and a better IS-ST.

(c) Simulated factors test results: Combined with simulation, some references were used on our AMOLED mobile display product with a good TFT hysteresis level. As shown in table 1, the tested IS-ST declines about 10% when the C_M3_VDD decreases about 49%. Similarly, the tested IS-ST declines about 9%, 12% and 3% when the TFT L, Vinit, and VGMP reduces about 6%, 33% and 3% respectively. There is a good match between the simulated ΔIds and the tested IS-ST. On account of the difficulties to decrease the TFT L and the VGMP, the mainly optimization methods for IS-ST mainly focused on the decrease of C_M3_VDD and Vinit.

Table 1. Simulated factors test results

Item		Simulated ΔIds	Tested IS-ST
C_M3_VDD	49%↓	11%↓	10%↓
TFT L	6%↓	9%↓	9%↓
Vinit	33%↓	16%↓	12%↓
VGMP	3%↓	4%↓	3%↓

4. Conclusion

All the solutions proposed above has been applied so as to achieve the IS-ST value decreasing from 8 JNCD to 5.5JNCD at 0s, while the simulated ΔIds decreases from 3.7% to 1.4%, as shown in table2.

Table 2. Product application results

Item	Sample1	Sample2
Design	-	*Shown in table 1*
Simulated ΔIds	*3.7%*	*1.4%*
Tested IS-ST	*8JNCD*	*5.5JNCD*

5. Acknowledge

We would like to thank all the development team members for their hard work on this project. This work was supported by BOE Technology Co., LTD.

Reference

[1]AMOLED Pixel Structures Compensating the Hysteresis of Poly-Si TFTs. Myoung-Hoon Jung, Inho Choi, Ohyun Kim, Hoon-Ju Chung. Electronic and Electrical Engineering Division, POSTECH, Pohang, Gyeongbuk, 790-784, KOREA. School of Electronic Engineering, Kumoh National Institute of Technology, Gumi, Gyeongbuk, 730-701, KOREA.

[2] A Novel Evaluation Method for Short-Residual Image of AMOLED Display Jintao Peng*, Kuanjun Peng*, Fangzhen Zhang*, Shuang Sun*, Jing Niu*, Tingting Zhou*, Yanan Niu*, Lubin Shi*, Jinyu Ren* Display Device Research Institute, BOE Technology Group Co., LTD., Beijing 100176, China